19-0712; Rev 0; 1/89

MAXIM

µP Compatible 14-Bit D/A Converter

General Description

The MX7536 is a high performance CMOS monolithic 14-bit digital-to-analog converter (DAC) that is optimized and specified to operate as a bipolar output part. Since the resistors required for 4-quadrant multiplying operation are included in the MX7536, only two op amps and a voltage reference are required externally. Wafer level laser trimmed thin-film resistors and temperature compensated NMOS switches assure specified performance over the full operating temperature ranges with exceptional linearity and gain stability.

The MX7536 is configured to operate with an 8- or 16-bit data bus with separate Most Significant (MS) and Least Significant (LS) byte chip select controls. In addition, all digital inputs are compatible with both TTL and 5V CMOS logic levels. The device is protected against CMOS "latchup" and does not require external Schottky protection diodes.

The MX7536 is available in 28-pin 600 mil wide DIP, PLCC or Small Outline (SO) packages.

Applications

Machine and Motion Control Systems

Automatic Test Equipment

Digital Audio

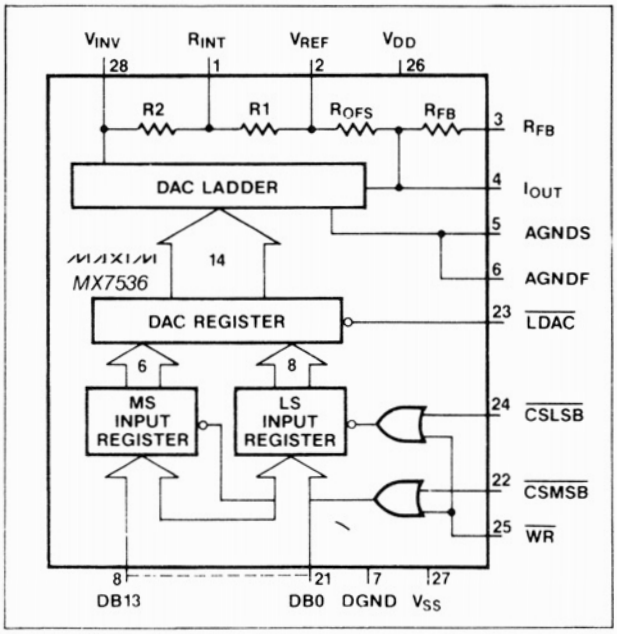
µP Controlled Calibration Circuitry

Programmable Gain Amplifiers

Digitally Controlled Filters

Programmable Power Supplies

Functional Diagram



Features

- 14-Bit Monotonic over Full Temperature Range
- Full 4-Quadrant Multiplication
- µP Compatible Double Buffered Inputs
- Exceptionally Low Gain Tempco (2ppm/°C)
- Low Output Leakage (<20nA) over the Full Temperature Range
- Low Power Consumption
- TTL and CMOS Compatible

Ordering Information

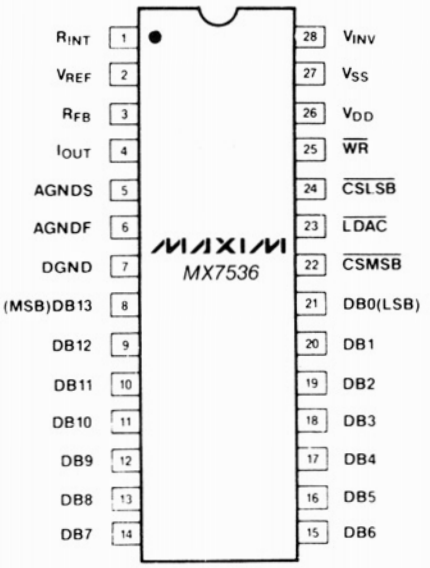
PART	TEMP. RANGE	PACKAGE*	ACCURACY
MX7536JN	0°C to +70°C	Plastic DIP	±2 LSB
MX7536KN	0°C to +70°C	Plastic DIP	±1 LSB
MX7536JCWI	0°C to +70°C	Wide SO	±2 LSB
MX7536KCWI	0°C to +70°C	Wide SO	±1 LSB
MX7536JP	0°C to +70°C	PLCC	±2 LSB
MX7536KP	0°C to +70°C	PLCC	±1 LSB
MX7536J/D	0°C to +70°C	Dice	±2 LSB
MX7536AQ	-25°C to +85°C	CERDIP	±2 LSB
MX7536BQ	-25°C to +85°C	CERDIP	±1 LSB
MX7536AD	-25°C to +85°C	Ceramic	±2 LSB
MX7536BD	-25°C to +85°C	Ceramic	±1 LSB

(Ordering information continued on page 10.)

**Maxim reserves the right to ship Ceramic in lieu of CERDIP packages.*

Pin Configuration

Top View



See page 10 for Plastic Chip Carrier Pin Configuration

µP Compatible 14-Bit D/A Converter

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to AGND ..... -15V, +0.3V
V_{REF} to AGND ..... ±25V
R_{FB} to AGND ..... ±25V
R_{INT} to AGND ..... ±25V
V_{INV} to AGND ..... ±25V
Digital Input Voltage (pins 8-25)
to DGND ..... -0.3V, V_{DD} +0.3V
V (pin 4) to DGND ..... -0.3V, V_{DD} +0.3V

AGND to DGND ..... -0.3V, V_{DD} +0.3V
Power Dissipation (any package) 1000mW
Derate above 75°C ..... 10mW/°C
Operating Temperature Ranges
MX7536J/K ..... 0°C to +70°C
MX7536A/B ..... -25°C to +85°C
MX7536S/T ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +11.4V to +15.75V (Note 1), V_{REF} = +10V, V_{AGNDF} = V_{AGNDS} = V_{SS} = 0V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				14			Bits
Relative Accuracy			MX7536K/B/T MX7536J/A/S			±1 ±2	LSB
Differential Non-Linearity		Guaranteed Monotonic Over Temperature	MX7536K/B/T MX7536J/A/S			±1	LSB
Full Scale Error		Measured with internal R_{FB} and includes effects of leakage current and gain T.C.	MX7536J/A/S MX7536K/B/T			±16 ±8	LSB
Offset Error		Error due to mismatch between R_{FB} and offset resistor. It also includes leakage current to I_{OUT} and is measured when the DAC is loaded with all 0s.				±4	LSB
Gain Temperature Coefficient (Note 2) ΔGain/ΔTemperature					±2	±5	ppm/°C
Offset Temperature Coefficient (Note 2) ΔOffset/ΔTemperature			MX7536J/A/S MX7536K/B/T		±1 ±1	±5 ±2.5	ppm/°C
INPUT RESISTANCES							
V_{REF} Input Resistance	R_{REF}			3	6	13	kΩ
V_{INV} Input Resistance	R_{INV}			2	4	8	kΩ
DIGITAL INPUTS							
Logic HIGH threshold	V_{INH}			+2.4			V
Logic LOW threshold	V_{INL}					+0.8	V
Input Leakage current		Digital inputs = 0V or V_{DD}	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	µA
Input Capacitance (Note 2)	C_{IN}					7	pF

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +11.4V to +15.75V (Note 1), V_{REF} = +10V, V_{AGNDF} = V_{AGNDS} = V_{SS} = 0V unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Positive Supply Range	V_{DD}	Accuracy Guaranteed	+11.4		+15.75	V
Negative Supply Range	V_{SS}	Accuracy Guaranteed	-200		-500	mV
Positive Supply Current	I_{DD}	Digital inputs = V_{INH} or V_{INL}			4	mA
		Digital inputs = 0V or V_{DD}			500	μA
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$		ΔV_{DD} = $V_{DD(MAX)}$ - $V_{DD(MIN)}$			±0.02	%/%

Note 1: Specifications are guaranteed for V_{DD} of +11.4V to +15.75V. At V_{DD} of 5V device is still functional with degraded specifications.

Note 2: Guaranteed by Product Assurance Testing.

AC PERFORMANCE CHARACTERISTICS

These are included for Design Guidance only and are not subject to test.
(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{AGNDS} = V_{AGNDF} = 0V. V_{SS} = 0V. Output Amplifier is AD544 unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Settling Time		T_A = 25°C To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s.		0.8	1.5	μsec
Digital to Analog Glitch Impulse		T_A = 25°C Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.		50		nV-sec
Multiplying Feedthrough Error (Note 3)		V_{REF} = ±10V, 1kHz sine wave DAC register loaded with 10 0000 0000 0000 T_A = 25°C		4		mV_{p-p}
Output Capacitance C_{OUT} (I_{OUT} pin) C_{OUT} (I_{OUT} pin)		T_A = T_{MIN}, T_{MAX} DAC register loaded with all 1s DAC register loaded with all 0s			260 130	pF
Output Noise Voltage Density (10Hz-100kHz)		Measured between R_{FB} and I_{OUT} T_A = 25°C		50		$nV/\sqrt{Hz}$

Note 3: Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

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TIMING CHARACTERISTICS

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{AGNDF} = V_{AGNDS} = 0V. V_{SS} = 0V. All specifications T_{MIN} to T_{MAX} unless otherwise noted. See Figure 1 for Timing Diagram.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time	t_1	T_A = -55°C to +125°C	0			ns
$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time	t_2	T_A = -55°C to +125°C	0			ns
$\overline{LDAC}$ Pulse Width	t_3	T_A = +25°C T_A = -25°C to +85°C T_A = -55°C to +125°C	170 200 240			ns
Write Pulse Width	t_4	T_A = +25°C T_A = -25°C to +85°C T_A = -55°C to +125°C	170 200 240			ns
Data Setup Time	t_5	T_A = +25°C T_A = -25°C to +85°C T_A = -55°C to +125°C	140 160 180			ns
Data Hold Time	t_6	T_A = +25°C T_A = -25°C to +85°C T_A = -55°C to +125°C	20 20 30			ns

Pin Description

Pin	Function	Description
1	R_{INT}	Junction point for internal R1 and R2 resistors which invert the V_{REF} with an external op amp.
2	V_{REF}	Reference input to DAC. It is internally connected to R_{OFS} and R1.
3	R_{FB}	Feedback Resistor. Used to close the loop around an external op amp.
4	I_{OUT}	Current Output
5	AGNDS	Analog Ground Sense. Reference point for external circuitry. This pin should carry minimum current.
6	AGNDF	Analog Ground Force. Carries current from internal analog ground connections. AGNDS and AGNDF are tied together internally.
7	DGND	Digital Ground
8	DB13	Data Bit 13 (MSB)
9	DB12	Data Bit 12
10	DB11	Data Bit 11
11	DB10	Data Bit 10
12	DB9	Data Bit 9
13	DB8	Data Bit 8
14	DB7	Data Bit 7
15	DB6	Data Bit 6
16	DB5	Data Bit 5
17	DB4	Data Bit 4
18	DB3	Data Bit 3
19	DB2	Data Bit 2
20	DB1	Data Bit 1
21	DB0	Data Bit 0 (LSB)
22	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte Active Low.
23	$\overline{LDAC}$	Asynchronous Load DAC input. Active Low.
24	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active Low.
25	$\overline{WR}$	Write input. Active Low.
26	V_{DD}	+12V to +15V supply voltage.
27	V_{SS}	Bias pin for high temperature low leakage configuration.
28	V_{INV}	This pin must be connected to the output of the external inverting op amp (Figure 5).

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Function
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load LS and MS Input Registers
1	1	0	X	Load DAC Register from Input Register
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE: X = Don't Care

Detailed Description

D/A Section

The basic MX7536 DAC circuit consists of a laser-trimmed, thin-film 11-bit R-2R resistor array, a 3-bit segmented resistor array, and NMOS current switches as shown in Figure 2. The three MSBs are decoded to drive the switches A-G of the segmented array, and the remaining bits drive switches S0-S10 of the R-2R array.

Binarily weighted currents are switched to either AGNDF or I_{OUT} depending on the status of each input bit. The R-2R ladder current is 1/8th of the total reference input current. The remaining 7/8th current flows into the segmented resistors dividing equally among these 7 resistors. The input resistance at V_{REF} is constant, and therefore, it can be driven by a voltage or current source of positive or negative polarity.

The MX7536 is optimized for bipolar output operation and uses the offset binary input coding. The R1 and R2 resistors are added to allow inversion of any reference voltage applied to the V_{REF} pin by using an external op amp. Furthermore, R_{OFS}, which is matched to R_{FB}, is added to offset the output by a constant $-V_{REF}$, resulting in offset binary coding.

Two separate analog ground pins, AGNDS and AGNDF, are provided to eliminate any variations in the ground potential as seen internally by the DAC. AGNDF is used to sink all current, while AGNDS is used to sense the internal ground potential. An amplifier, A3, can be optionally used to force the internal DAC ground to the system's analog ground potential as shown in Figure 2. AGNDF and AGNDS connections may be changed to accommodate the required output drive and system accuracy.

The equivalent circuit for the DAC is shown in Figure 3. C_{OUT} varies from typically 90pF to 180pF depending on the digital code. R_O denotes the equivalent output resistance of the DAC which varies with input code. $g(V_{REF},N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the digital input code of the DAC, N.

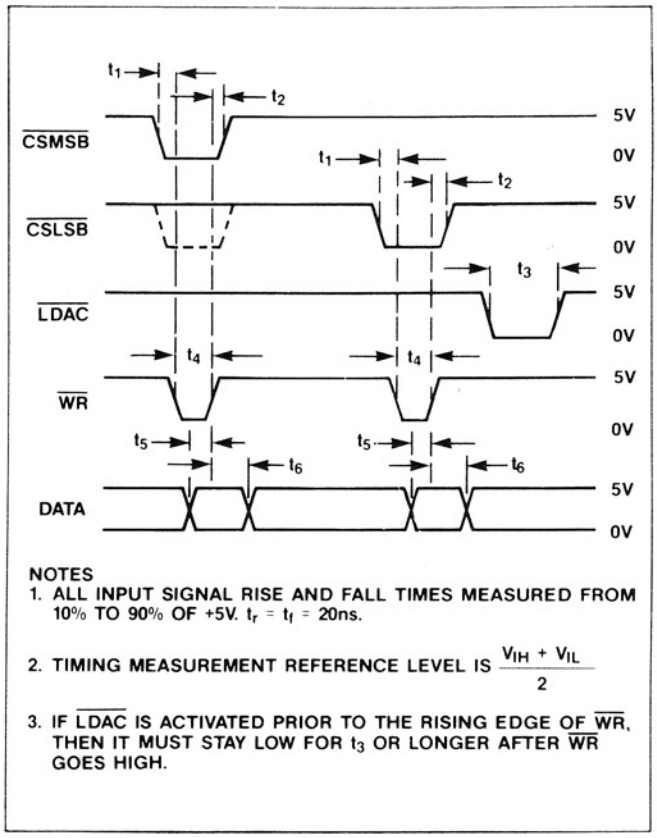

Figure 1. MX7536 Timing Diagram

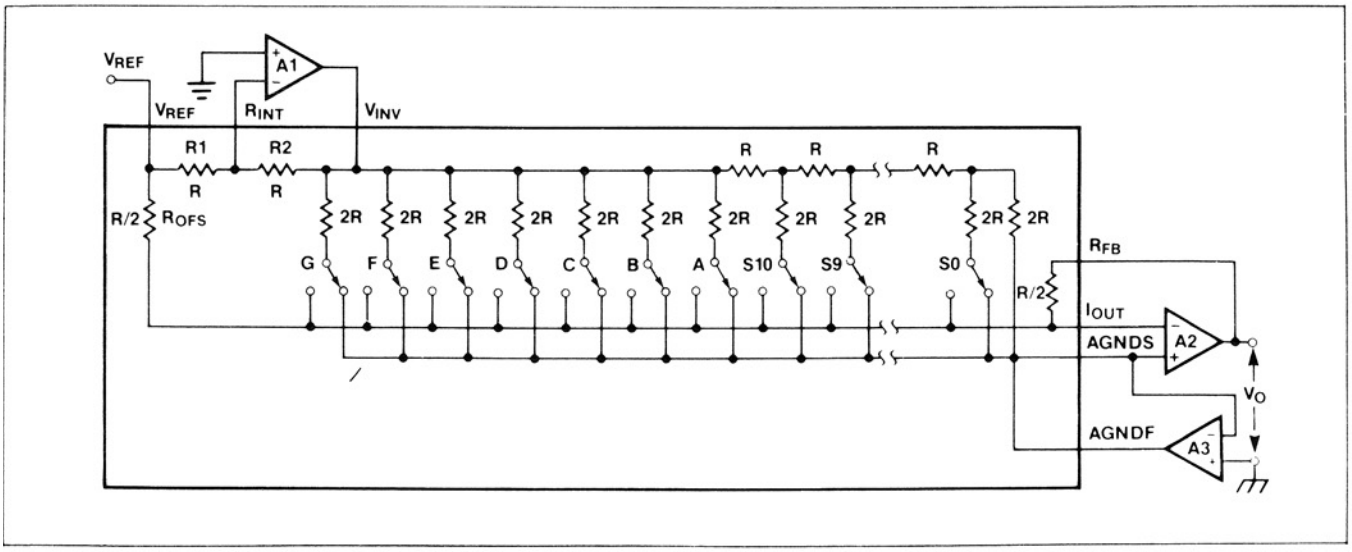

Figure 2. Simplified Circuit Diagram of the MX7536 D/A Section Showing Connection of External Op Amps

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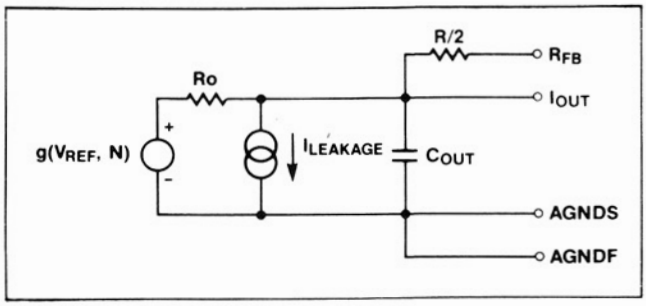

Figure 3. Equivalent Analog Output Circuit

Digital Section

All digital inputs are both TTL and 5V CMOS logic compatible. All inputs are protected for electrostatic discharge and have typical input currents of less than 1nA. Supply current will be minimized when the digital input voltages are kept as close to 0V and 5V levels as possible.

Application Information

Bipolar Operation for MX7536 (4-Quadrant Multiplication)

The MX7536 is a dedicated bipolar DAC. Specified accuracy is obtained without the use of expensive closely matched external resistors. As shown in Figure 4, R1 and R2 provide an optional gain adjustment, and capacitor C1 helps prevent overshoot and ringing when high speed op amps are used. In this circuit AGNDF and AGNDS are externally shorted to ground. Generally, another op amp is used to Kelvin the ground connection as shown in Figure 5.

Table 1 shows the Offset Binary Code obtained with the circuit of Figure 5. Note that by inverting the MSB of the DAC word, 2's Complement transfer function can be obtained.

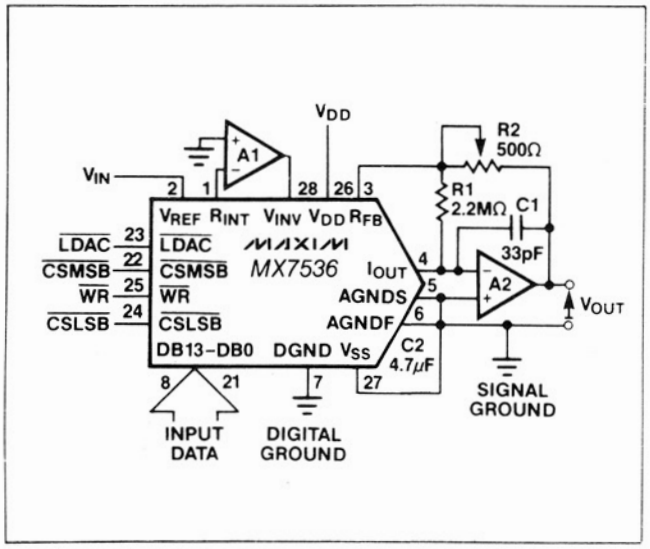

Figure 4. MX7536 Operation

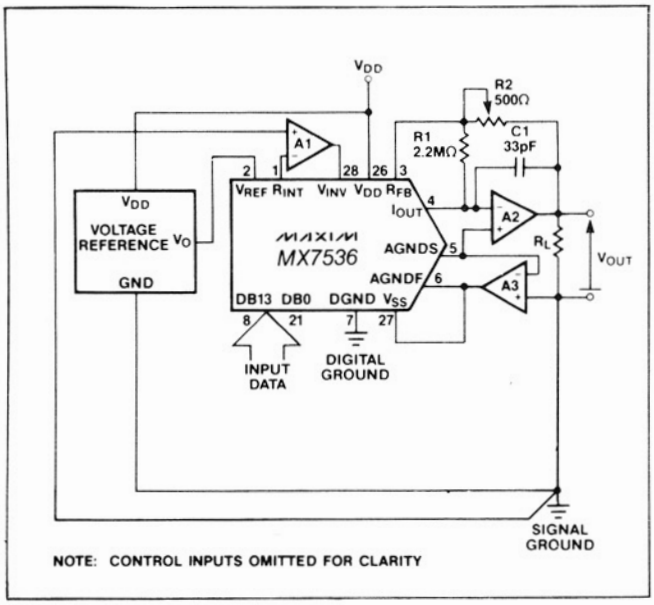

Figure 5. MX7536 Operation with Forced Ground

Offset and Gain Adjustment of MX7536

Offset Adjustment

1. Adjust offset of amplifier A1 so that potential at R_{INT} is $<10\mu V$ with respect to signal ground.
2. Load DAC register with all 0s.
3. Adjust offset of amplifier A2 until $V_{OUT} = -V_{IN} \pm 10\mu V$.

Gain Adjustment

1. Load DAC register with all 1s.
2. Trim potentiometer R2 so that $V_{OUT} = +V_{IN}$ (8191/8192)

For wide temperature range applications, resistors and potentiometers should have low temperature coefficients. In many applications by virtue of the excellent temperature coefficients of the offset and gain errors of the MX7536, adjustments may not be needed.

Grounding Considerations

Since I_{OUT} and the output amplifier's noninverting input are sensitive to offset voltages, nodes that need to be grounded should be connected directly to a "single point" ground through a separate, very low resistance path. Note that the output current at I_{OUT} and AGNDF vary with input code and create a code dependent error if these terminals are connected to ground (or a virtual ground) through a resistive path.

It is important to use a proper grounding technique to obtain high accuracy. The two AGND pins (AGNDF, AGNDS) provide flexibility in this respect. In Figure 4, AGNDS and AGNDF are shorted together externally and an extra op amp, A2, is not required. Voltage drops due to bond wire resistance are not compensated for in this circuit. This could create a linearity error (about 0.1LSB due to bond wire resistance

alone) which can be eliminated by using the circuit of Figure 5. Here A2 maintains AGNDS at signal ground potential. By using Force/Sense techniques all switch contacts on the DAC are kept at exactly the same potential and any error due to bond wire resistance is eliminated.

Figure 6 is a suggested printed circuit board (PCB) layout for the MX7536.

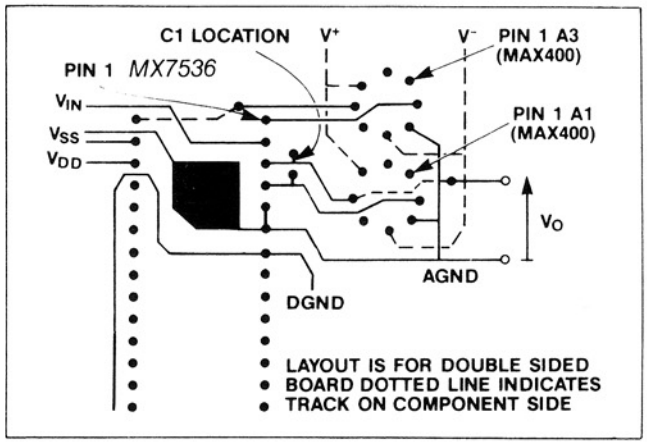

Figure 6. Suggested Layout for MX7536 Circuit of Figure 4

Low Leakage Configuration

Leakage currents in the DAC flowing into the I_{OUT} line can cause gain, linearity and offset errors. Leakage is worse at high temperatures.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must settle quickly to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic signal coupling from the V_{REF} terminal to I_{OUT}. This is normally a function of board layout and lead-to-lead package capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

Compensation

A compensation capacitor, C1, may be needed when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. Its value depends on the type of op amp used. Typical values range from 10pF to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized, and output settling performance improved, by keeping the PC board trace and stray capacitance at I_{OUT} as small as possible.

Bypassing

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected as close to the DAC's V_{DD} and GND pins as possible. High frequency noise rejection is optimized if tantalum is used for the 1μF capacitor. V_{SS} decoupling capacitor of 4.7μF is also required if low leakage configuration is used.

The MX7536 has high-impedance digital inputs. To minimize noise pick-up, they should be connected to either V_{DD} or GND terminals when not used. It is also good practice to connect active inputs to V_{DD} or GND through high valued resistors (1MΩ) to prevent static charge accumulation if these pins are left floating, as might be the case when a circuit card is left unconnected.

Op Amp Selection

Input offset voltage (V_{OS}), input bias current (I_B) and offset voltage drift (tempco of V_{OS}) are three key parameters determining the choice of a suitable amplifier. To maintain specified accuracy with V_{REF} of 10V, V_{OS} should be less than 30μV, and I_B should be less than 2nA. Open loop gain should be greater than 100,000. Maxim's MAX400 has low V_{OS} (10μV max), low I_B (2nA) and low TC V_{OS} (0.03μV/°C max). This op amp can be used without requiring any adjustments. For medium frequency applications, the OP-27 and for even higher frequency applications the HA-2620 are recommended. However these op amps require external offset adjustment (Table 1).

Table 1. Amplifier Performance Comparisons

OP AMP	INPUT OFFSET VOLTAGE (V_{OS})	INPUT BIAS CURRENT (I_B)	OFFSET VOLTAGE DRIFT (TC V_{OS})	SETTLING TO 0.003% FS
MAX400M	10μV	2nA	0.03μV/°C	50μs
Maxim OP-07A	25μV	2nA	0.06μV/°C	50μs
AD544L	500μV	25pA	5μV/°C	5μs
HA2620	4mV	35nA	20μV/°C	0.8μs

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Microprocessor Interfacing

8086A

Interfacing is possible to both 8- and 16-bit processors. Figure 7 shows the 8086 16-bit processor interfacing to a single MX7536. In this setup the double buffering feature of the DAC is not used. AD0-AD13 of the 16-bit data bus are connected to the DAC data bus (DB0-DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000 (HEX). A software routine for Figure 7 is given in Table 2.

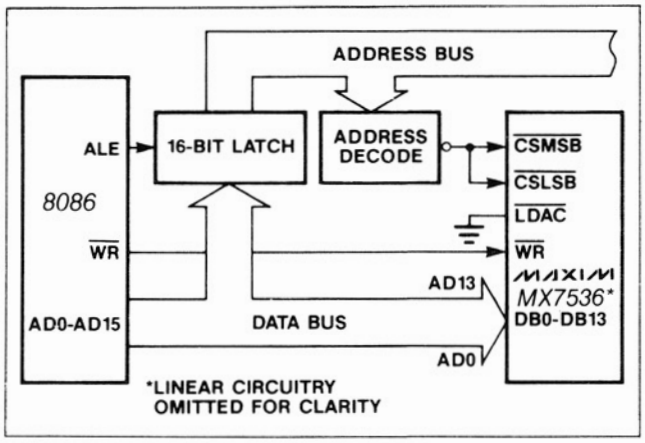

Figure 7. MX7536-8086 Interface Circuit

In a multiple DAC system the double buffering of the DAC allows the user to simultaneously update all DACs. In Figure 8, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., LDAC) is brought low, updating all the DACs simultaneously.

MC68000

Figure 9 shows an interface diagram. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

```
01000 MOVE.W  #W,D0      : The desired DAC data, W, is
                           loaded into Data Register 0.
      MOVE.W  D0,$E000   : The Data W is transferred
                           between D0 and DAC register.
      MOVE.B  #228,D7    : Control returned to the
                           System Monitor Program.
      TRAP    #14
```

Z80 Interface

The MX7536 is ideally suited to being used with 16-bit processors or in stand-alone applications. However, it can be used with an 8-bit processor as shown in the example circuit of Figure 10, an interface circuit for the Z80.

Digital Feedthrough

In the interface diagrams shown in Figures 7 to 10, the digital inputs of the DAC are directly connected to the microprocessor bus. Even when the device is not selected, activity on the bus can feedthrough to the DAC output through package capacitance and shows up as noise. This can be minimized by isolating the DAC from the digital bus as shown in Figure 11.

Table 2. Sample Program for Loading MX7536

		ASSUME DS:DACLOAD,CS:DACLOAD DACLOAD SEGMENT AT 000	
00	8CC9	MOV CX,CS	:DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOVDS,CX	:TO CODE SEGMENT REGISTER
04	BF00D0	MOVDI,#D000	:LOAD DI WITH D000
07	C705"YZWX"	MOV MEM,#YZWX	:DAC LOADED WITH WXYZ
0B	EA0000		:CONTROL IS RETURNED TO THE
0E	00FF		MONITOR PROGRAM

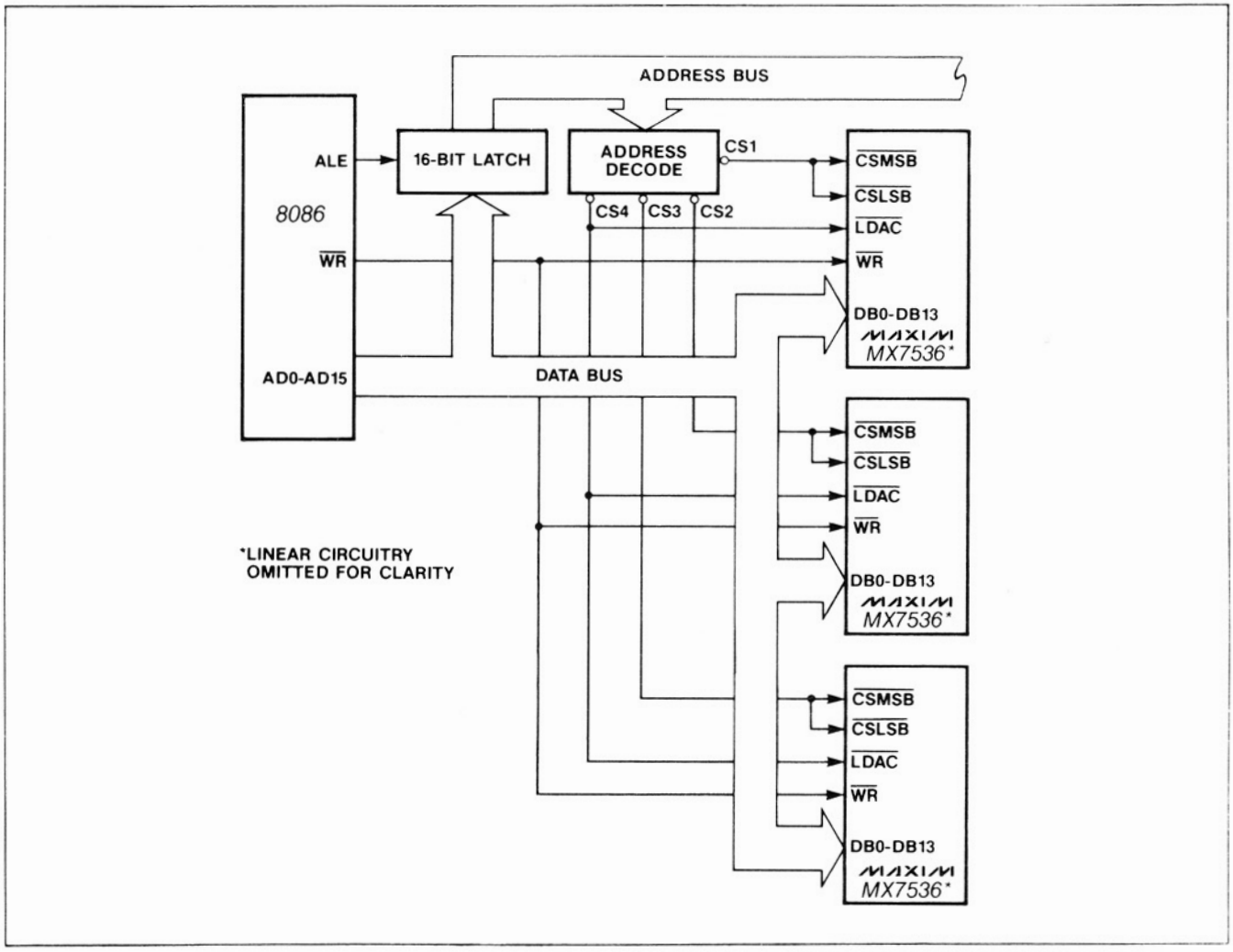

Figure 8. MX7536-8086 Interface: Multiple DAC System

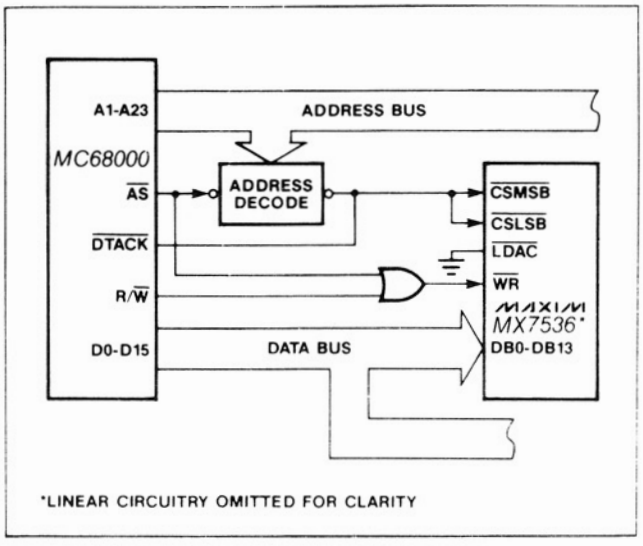

Figure 9. MX7536-MC68000 Interface

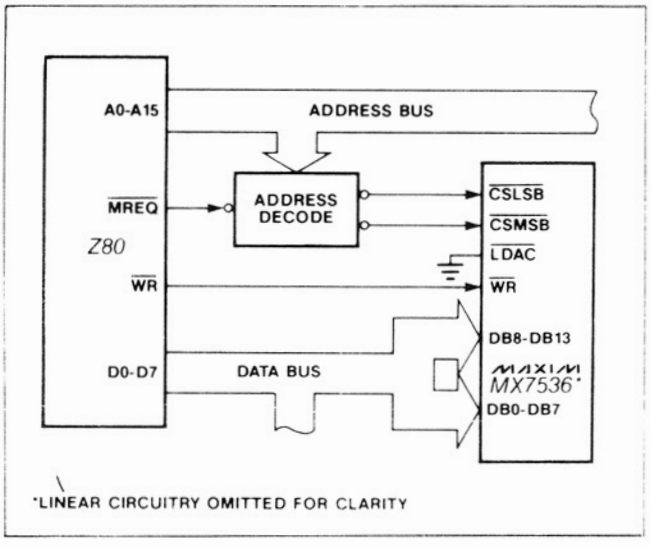

Figure 10. MX7536-Z80 Interface

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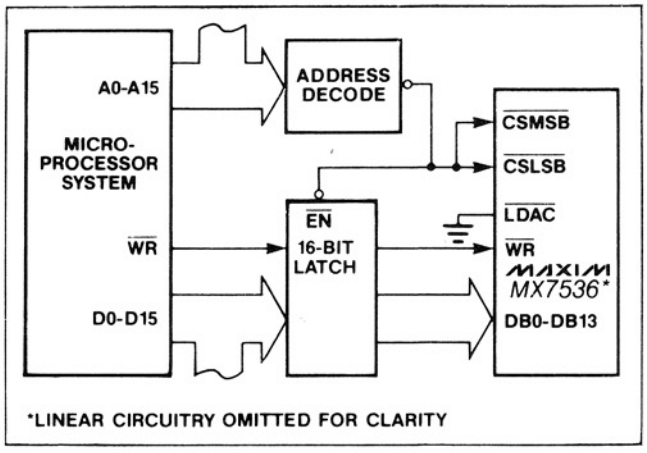


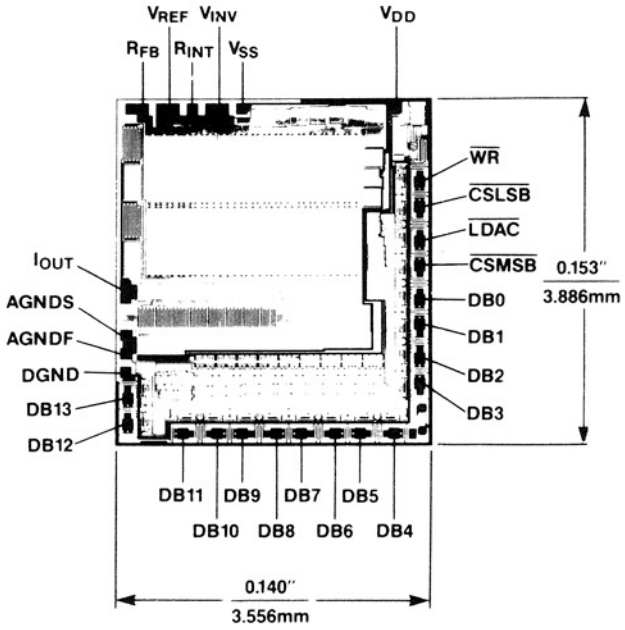
Figure 11. MX7536 Interface Circuit Using Latches to Minimize Digital Feedthrough

Ordering Information (continued)

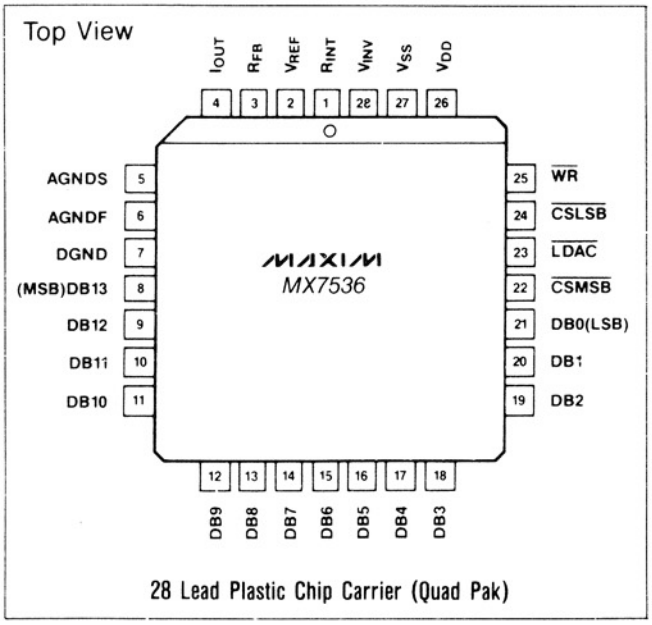
PART	TEMP. RANGE	PACKAGE*	ACCURACY
MX7536SQ	-55°C to +125°C	CERDIP	±2 LSB
MX7536TQ	-55°C to +125°C	CERDIP	±1 LSB
MX7536SD	-55°C to +125°C	Ceramic	±2 LSB
MX7536TD	-55°C to +125°C	Ceramic	±1 LSB

***Maxim reserves the right to ship Ceramic in lieu of CERDIP packages.**

Chip Topography

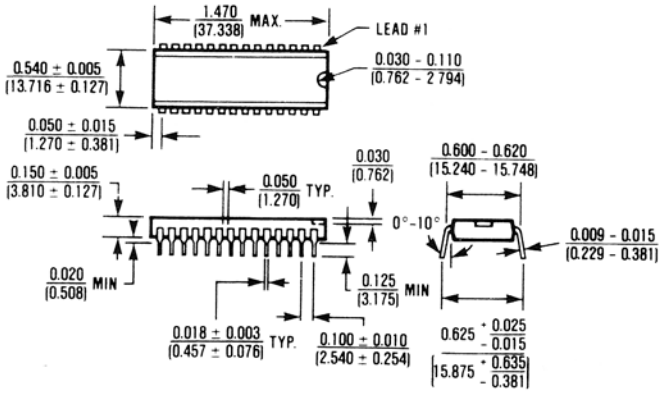


Pin Configuration (continued)



Package Information

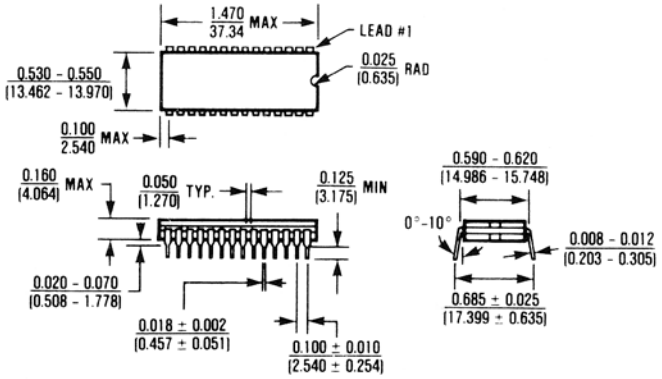
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



28 Lead Plastic DIP (PI)

θ_{JA} = 110°C/W

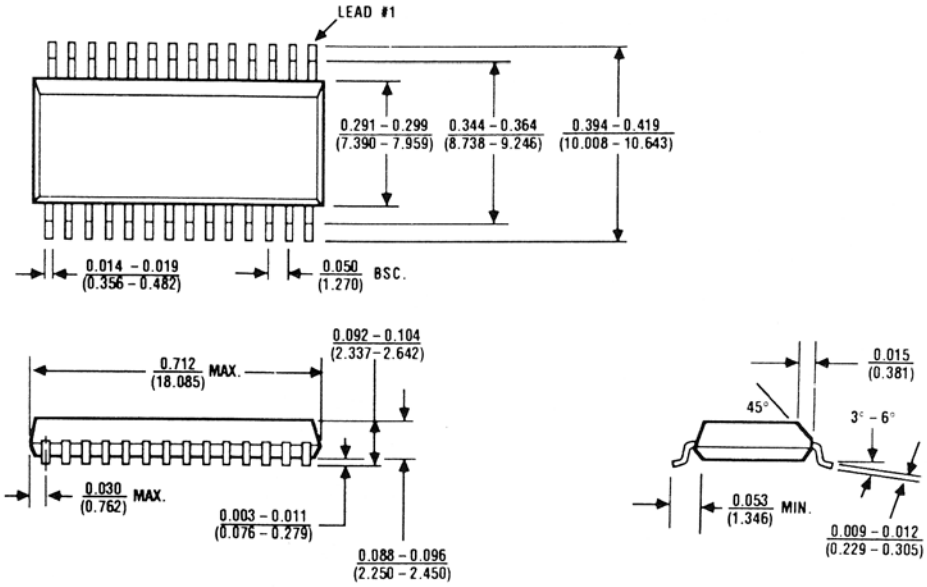
θ_{JC} = 50°C/W



28 Lead CERDIP (JI)

θ_{JA} = 55°C/W

θ_{JC} = 20°C/W



28 Lead Small Outline, Wide (WI)

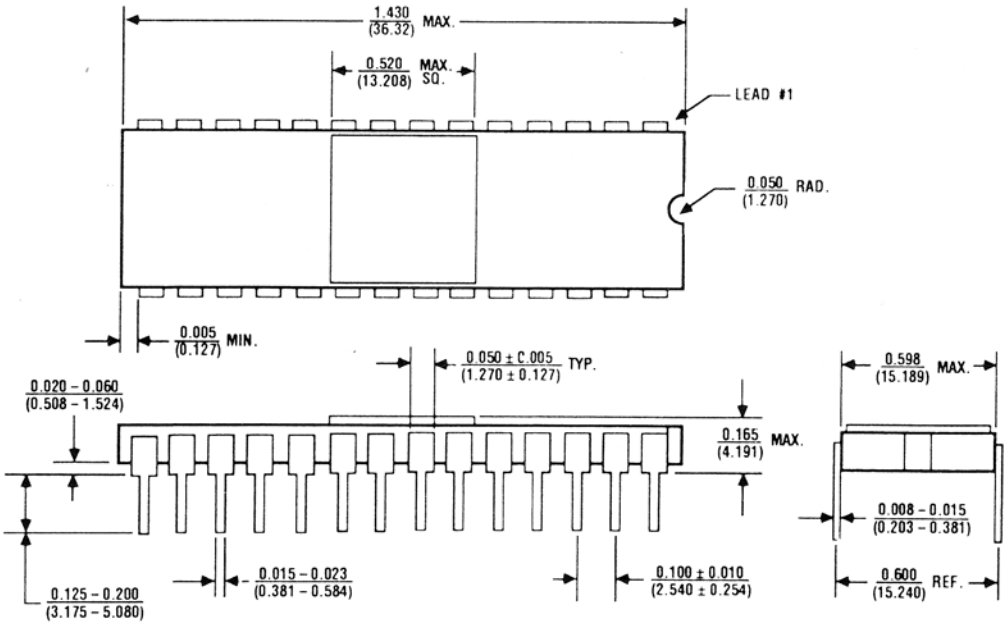
θ_{JA} = 80°C/W

θ_{JC} = 45°C/W

µP Compatible 14-Bit D/A Converter

Package Information (continued)

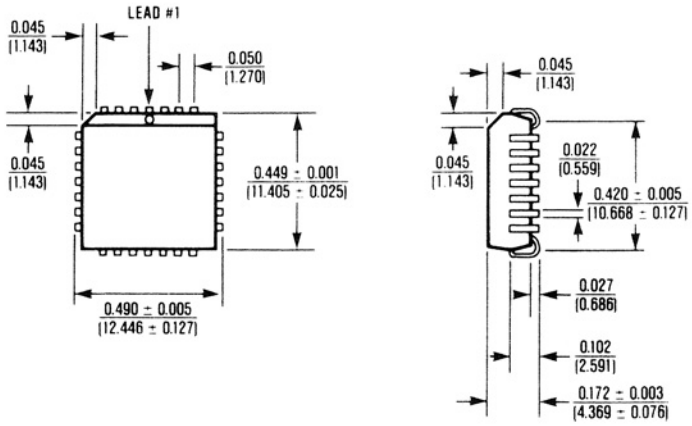
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



28 Lead Ceramic Sidebraze (DI)

θ_{JA} = 50°C/W

θ_{JC} = 15°C/W



28 Lead Plastic Chip Carrier (Quad Pak) (QI)

θ_{JA} = 100°C/W

θ_{JC} = 45°C/W